14.0 DIFFERENCES BETWEEN MILITARY INTEL486 PROCESSORS AND INTEL386 PROCESSORS

The differences between Military Intel486 processors and Intel386 processors are due to performance enhancements. The differences are listed below.

1. Instruction clock counts have been reduced to achieve higher performance. (See section 13.0, ''Instruction Set Summary.'')
2. The Military Intel486 processor bus is significantly faster than the Intel386 processor bus. Differences include a 1X clock, parity support, burst cycles, cacheable cycles, cache invalidate cycles and 8-bit bus support. The Hardware Interface and Bus Operation sections (sections 9.0 and 10.0) of the data sheet should be carefully read to understand the Military Intel486 processor bus functionality.
3. To support the on-chip cache bits have been added to control register 0 (CD and NW) (see section 4.2.3.1, ''Control Registers''), new pins have been added to the bus (see section 9.0, ''Hardware Interface'') and new bus cycle types have been added (see section 10.0, ''Bus Operation''). The on-chip cache needs to be enabled after reset by clearing the CD and NW bit in CR0.
4. Eight new instructions have been added:
   - Byte Swap (BSWAP)
   - Exchange-and-Add (XADD)
   - Compare and Exchange (CMPXCHG)
   - Invalidate Data Cache (INVD)
   - Write-back and Invalidate Data Cache (WBINVD)
   - Invalidate TLB Entry (INVLPG)
   - Processor Identification (CPUID)
   - Resume (RSM)
5. Two bits defined in control register 3, the page table entries and page directory entries (PCD and PWT). (See section 6.4.2.5, ''Page Directory/Table Entries.'')
6. A page protection feature has been added. This feature required a new bit in control register 0 (WP) (See sections 4.2.3.1 ''Control Registers'' and 6.4.3 ''Page Level Protection.'')
7. An Alignment Check feature has been added. This feature required a bit in the flags register (AC) (section 4.2.2.3 ''Flags Register'') and a bit in control register 0 (AM) (section 4.2.3.1 ''Control Registers'').
8. The replacement algorithm for the translation lookaside buffer has been changed from a random algorithm to a pseudo least recently used algorithm like that used by the on-chip cache. (See section 7.5 ''Cache Replacement'' for a description of the algorithm.)
9. Three testability registers, TR3, TR4 and TR5, have been added for testing the on-chip cache. TLB testability has been enhanced. (See section 11.0, ''Testability.'')
10. The prefetch queue has been increased from 16 bytes to 32 bytes. A jump always needs to execute after modifying code to guarantee correct execution of the new instruction.
11. After reset, the ID in the upper byte of the DX register is 04.

14.1 Differences between the Intel386 Processor with an Intel387™ Math CoProcessor and Military Intel486 DX, IntelDX2 and IntelDX4 Processors

In addition to the previously mentioned enhancements, the Military Intel486 DX, IntelDX2 and IntelDX4 processors offer the following features:

1. The complete Intel387 math coprocessor instruction set and register set have been added. No I/O cycles are performed during Floating Point instructions. The instruction and data pointers are set to 0 after FINIT/FSAVE. Interrupt 9 can no longer occur, interrupt 13 occurs instead.
2. Support for floating point error reporting modes to guarantee DOS compatibility. These modes require a bit in control register 0 (NE) (see section 4.2.3.1, ''Control Registers'') and pins (FERR# and IGNNE#). (See sections 9.2.15, ''Numeric Error Reporting'' and 10.2.14 ''Floating Point Error Handling.'')
3. In some cases FERR# is asserted when the next floating point instruction is encountered and in other cases it is asserted before the next floating point instruction is encountered, depending upon the execution state the instruction causing exception. (See sections 9.2.15, ''Numeric Error Reporting'' and 10.2.14, ''Floating Point Error Handling.'') For both of these cases, the Intel387 math coprocessor asserts ERROR# when the error occurs and does not wait for the next floating point instruction to be encountered.
4. The contents of the base registers ***including the floating point registers*** may be different after reset.

15.0 ELECTRICAL DATA

The following sections describe recommended electrical connections and electrical specifications for the Military Intel486 processor.

15.1 Power and Grounding

15.1.1 POWER CONNECTIONS

The Military Intel486 processor is implemented in CHMOS technology and has modest power requirements. However, the high clock frequency output buffers can cause power surges as multiple output buffers drive new signal levels simultaneously. For clean on-chip power distribution at high frequency, multiple V_{CC} and V_{SS} pins feed the Military Intel486 processor.

Power and ground connections must be made to all external V_{CC} and GND pins of the Military Intel486 processor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must be likewise connected on a GND plane.

15.1.2 MILITARY INTEL486 PROCESSOR POWER DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Military Intel486 processor. The Military Intel486 processor, driving its 32-bit parallel address and data buses at high frequencies, can cause transient power surges, particularly when driving large capacitive loads. Low inductance capacitors (i.e., surface-mount capacitors) and interconnects are recommended for the best high-frequency electrical performance. Inductance can be reduced by connecting capacitors directly to the V_{CC} and V_{SS} planes, with minimal trace length between the component pads and vias to the plane. These capacitors should be evenly distributed around each component on the V_{CC} power plane.

Capacitor values should be chosen to ensure they eliminate both low and high frequency noise components.

The recommendation for the Military Intel486 processor is 9 x 0.01 μF and 9 x 0.1 μF capacitors.

The power consumption can transition from a low level of power to a much higher level (or high to low power) very rapidly. A typical example would be entering or exiting the Stop Grant state. Another example would be executing a HALT instruction, causing the Military Intel486 processor to enter the Auto HALT Power Down state, or transitioning from HALT to the Normal state. All of these examples may cause abrupt changes in the power being consumed by the Military Intel486 processor. Bulk storage capacitors with a low ESR (Effective Series Resistance) in the 10 to 100 microfarad range are required to maintain a regulated supply voltage during the interval between the time the current load changes and the point that the regulated power supply output can react to the change in load. In order to reduce the ESR, it may be necessary to place several bulk storage capacitors in parallel. These capacitors should be placed near the Military Intel486 processor (on the processor power plane) to ensure that the supply voltage stays within specified limits during changes in the supply current while in operation.

15.1.3 V_{CC5} AND V_{CC} POWER SUPPLY REQUIREMENTS FOR THE INTELDX4 PROCESSOR

In mixed voltage systems that will be driving IntelDX4 processor inputs in excess of 3.3V, the V_{CC5} pin must be connected to the system 5V supply. In order to limit current flow into the V_{CC5} pin, there is a limit to the voltage differential between the V_{CC5} pin and the other V_{CC} pins. The voltage differential between the V_{CC5} pin of the IntelDX4 processor and its 3.3V V_{CC} pins should never exceed 2.25V. The 2.25V limit applies to power up, power down and steady state operation. Table 15-1 outlines this requirement.

Table 15-1. Dual Power Supply Requirements for the IntelDX4™ Processor

Symbol	Parameter	Min	Max	Unit	Notes
VDIFF	V_{CC5}–V_{CC} Difference		2.25	V	V_{CC5} input should not exceed V_{CC} by more than 2.25V during power-up, power-down or during operation.

Meeting this requirement ensures proper operation of the IntelDX4 processor and guarantees that the current draw into the V_{CC5} pin will not exceed the I_{CC5} specification (see section 15.3, ''DC Specifications''). If the voltage difference requirement cannot be met due to system design limitations, then an alternate solution may be employed. A minimum of a 100Ω series resistor may be used to limit the current into the V_{CC5} pin. This resistor will ensure that current drawn by the V_{CC5} pin will not exceed the maximum rating of 55 mA for this pin (see section 15.2, ''Maximum Ratings'').

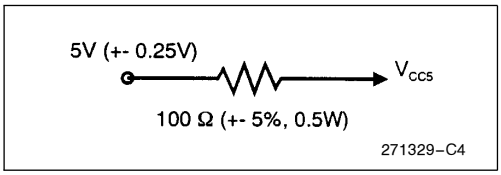

Figure 15-1. IntelDX4™ Processor V_{CC5} Current Limiting Resistor

Note that this resistor is not necessary if the system can guarantee that the voltage difference between V_{CC5} and V_{CC} is always limited to 2.25V, even during power up and power down.

In 3.3V-only systems and systems that will be driving all IntelDX4 processor inputs and I/Os from 3.3V logic, the V_{CC5} pin should be connected directly to the 3.3V V_{CC} plane. This will guarantee the voltage difference specification is met and will eliminate the current draw into the V_{CC5} pin. In a 3.3V-only system, the V_{CC5} may be connected to the 5V supply as described previously, as long as the voltage differential in Table 15-1 is met, and assuming the current drawn by the V_{CC5} pin is of little consequence to the system design.

15.1.4 SYSTEM CLOCK RECOMMENDATIONS

It is recommended that the CLK input to the Military Intel486 processor should not be driven until V_{CC} has reached its normal operating level (either 3.3V or 5V). The CLK input may be grounded or allowed to ramp with V_{CC} during this period. Once V_{CC} has reached its normal operating level, the Military Intel486 processor can handle the clock frequency for which it is specified and the oscillator/clock driver should have locked onto its desired frequency.

15.1.5 OTHER CONNECTION RECOMMENDATIONS

NC pins should always remain unconnected. Connection of NC pins to V_{CC} or V_{SS} or to any other signal can result in component malfunction or incompatibility with other steppings of the Military Intel486 processor family.

For reliable operation, always connect unused inputs to an appropriate signal level. Active LOW inputs should be connected to V_{CC} through a pull-up resistor. Pull-ups in the range of 20 KΩ are recommended. Active HIGH inputs should be connected to GND.

15.2 Maximum Ratings

Table 15-2 is a stress rating only. Functional operation at the maximums is not guaranteed. Function operating conditions are given in Table 15-3 for 3.3V processor DC Specifications, Table 15-5 for 5V DC Specifications, Tables 15-8 and 15-9 for 3.3V processor AC specifications, and Table 15-11 for 5V processor AC specifications.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the Military Intel486 processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 15-2. Absolute Maximum Ratings

Case Temperature under Bias	−65°C to +125°C
Storage Temperature	−65°C to +150°C
DC Voltage on Any Pin with Respect to Ground	−0.5 to V_{CC} + 0.5V −0.5 to V_{CC5} + 0.5V(1)
Supply Voltage with Respect to V_{SS}	V_{CC} −0.5V to +6.5V(2) V_{CC} −0.5V to +4.6V(1) V_{CC5}(1) −0.5V to +6.5V(1)
Transient Voltage on Any Input	−1.6V to V_{CC5} +1.6V(1,3)
Maximum Allowable Current Sink on V_{CC5}(1)	55 mA

NOTES:
1. For IntelDX4™ processor only.
2. All Military Intel486™ processors except IntelDX4 processor.
3. Maximum voltage on any pin with respect to ground is the lesser of Vcc5 + 1.6V or 6.5V for the IntelDX4 processor.

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15.3 DC Specifications

15.3.1 3.3V DC CHARACTERISTICS

Table 15-3 is for IntelDX4 processors.

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**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 15-3. 3.3V DC Specifications

Functional operating range: V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 7); T_{CASE} = −55°C to +125°C

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input LOW Voltage	−0.3		+0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC5}+0.3	V	
V_{IHC}	Input HIGH Voltage of CLK	V_{CC}−0.6		V_{CC}+0.3	V	
V_{OL}	Output LOW Voltage I_{OL} = 2.0 mA I_{OL} = 100 μA			 0.40 0.20	 V V	
				0.45	V	
V_{OH}	Output HIGH Voltage I_{OH} = −2.0 mA	 2.4			 V	
I_{CC5}	V_{CC5} Leakage Current		15	300	μA	
I_{LI}	Input Leakage Current			±15	μA	
I_{IH}	Input Leakage Current			200	μA	
I_{IL}	Input Leakage Current			−400	μA	
I_{LO}	Output Leakage Current			±15	μA	
C_{IN}	Input Capacitance			10	pF	
C_{OUT}	Output or I/O Capacitance			14	pF	6
C_{CLK}	CLK Capacitance			12	pF	

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Table 15-4. 3.3V I_{CC} Values for IntelDX4™ Processor

Functional Operating Range: $V_{CC} = 3.3V \pm 5\%$; $V_{CC5} = 5V \pm 0.25V$ (Note 7); $T_{CASE} = -55°C$ to $+125°C$

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	100 MHz 75 MHz		1450 mA 1100 mA	1
I_{CC} Active (Thermal Design)	100 MHz 75 MHz	1075 mA 825 mA	1300 mA 975 mA	2, 3, 4
I_{CC} Stop Grant	100 MHz 75 MHz	50 mA 20 mA	100 mA 75 mA	5
I_{CC} Stop Clock	0 MHz	600 μA	1 mA	6

NOTES:
1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at $V_{CC} = 3.465V$.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at $V_{CC} = 3.3V$.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at $V_{CC} = 3.3V$, running Microsoft Windows 3.1 at an idle condition. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I_{CC} Stop Grant specification refers to the I_{CC} value once the Military Intel486 processor enters the Stop Grant or Auto HALT Power Down state.
6. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specifications.
7. V_{CC5} should be connected to $3.3V \pm 5\%$ in 3.3V-only systems.

15.3.2 5V DC CHARACTERISTICS

Table 15-5 is for Military Intel486™ DX and IntelDX2 Processors.

Table 15-5. 5V DC Specifications

Functional operating range: V_{CC} = 5V ± 0.25V; T_{CASE} = −55°C to +125°C

Symbol	Parameter	Min	Typ	Max	Unit	Notes
V_{IL}	Input LOW Voltage	−0.3		+0.8	V	7
V_{IH}	Input HIGH Voltage	2.0		V_{CC}+0.3	V	8
V_{OL}	Output LOW Voltage			0.45	V	1
V_{OH}	Output HIGH Voltage	2.4			V	2
I_{LI}	Input Leakage Current			±15	μA	3
I_{IH}	Input Leakage Current			200	μA	4
I_{IL}	Input Leakage Current			−400	μA	5
I_{LO}	Output Leakage Current			±15	μA	
C_{IN}	Input Capacitance PGA			20	pF	6
C_{OUT}	Output or I/O Capacitance PGA			20	pF	6
C_{CLK}	CLK Capacitance PGA			20	pF	6

NOTES:
1. This parameter is measured at: Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at: Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
3. This parameter is for inputs without pull-ups or pull-downs and $0V \leq V_{IN} \leq V_{CC}$.
4. This parameter is for inputs with pull-downs and V_{IH} = 2.4V.
5. This parameter is for inputs with pull-ups and V_{IL} = 0.45V.
6. F_C=1 MHz; Not 100% tested.
7. Minimum value guaranteed by design characterization but not tested.
8. Maximum value guaranteed by design characterization but not tested.

Table 15-6. 5V I_{CC} Values for Military Intel486™ DX Processor

Functional Operating Range: $V_{CC} = 5V \pm 0.25V$; $T_{CASE} = -55°C$ to $+125°C$

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	33 MHz 25 MHz		900 mA 700 mA	1
I_{CC} Active (Thermal Supply)	33 MHz 25 MHz	700 mA 550 mA	857 mA 666 mA	2, 3, 4
I_{CC} Stop Grant	33 MHz 25 MHz	40 mA 40 mA	80 mA 80 mA	5
I_{CC} Stop Clock	0 MHz	200 μA	2 mA	6

Table 15-7. 5V I_{CC} Values for IntelDX2™ Processor

Functional Operating Range: $V_{CC} = 5V \pm 0.25V$; $T_{CASE} = -55°C$ to $+125°C$

Parameter	Operating Frequency	Typ	Maximum	Notes
I_{CC} Active (Power Supply)	50 MHz 66 MHz		950 mA 1200 mA	1
I_{CC} Active (Thermal Supply)	50 MHz 66 MHz	775 mA 975 mA	906 mA 1145 mA	2, 3, 4
I_{CC} Stop Grant	50 MHz 66 MHz	35 mA 45 mA	70 mA 90 mA	5
I_{CC} Stop Clock	0 MHz	200 μA	2 mA	6

NOTES:

1. This parameter is for proper power supply selection. It is measured using the worst case instruction mix at $V_{CC} = 5.25V$.
2. The maximum current column is for thermal design power dissipation. It is measured using the worst case instruction mix at $V_{CC} = 5V$.
3. The typical current column is the typical operating current in a system. This value is measured in a system using a typical device at $V_{CC} = 5V$, running Microsoft Windows 3.1 at an idle condition at room temperature. This typical value is dependent upon the specific system configuration.
4. Typical values are not 100% tested.
5. The I_{CC} Stop Grant specification refers to the I_{CC} value once the Military Intel486 processor enters the Stop Grant or Auto HALT Power Down state.
6. The I_{CC} Stop Clock specification refers to the I_{CC} value once the processor enters the Stop Clock state. The V_{IH} and V_{IL} levels must be equal to V_{CC} and 0V, respectively, in order to meet the I_{CC} Stop Clock specifications.

15.4 AC Specifications

The AC specifications given in the tables in this section consist of output delays, input setup requirements and input hold requirements. All AC specifications are relative to the rising edge of the input system clock (CLK) unless otherwise specified.

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15.4.1 3.3V AC CHARACTERISTICS

Table 15-8. 3.3V AC Characteristics for the 75/25-MHz IntelDX4™ Processor

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	25	MHz		2
t_1	CLK Period	40	125	ns	15-2	
t_{1a}	CLK Period Stability		±250	ps		3, 6
t_2	CLK High Time	14		ns	15-2	at 2V
t_3	CLK Low Time	14		ns	15-2	at 0.8V
t_4	CLK Fall Time		4	ns	15-2	2V to 0.8V
t_5	CLK Rise Time		4	ns	15-2	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA Valid Delay	2	19	ns	15-6	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		28	ns	15-7	3
t_8	PCHK# Valid Delay	2	24	ns	15-5	
t_{8a}	BLAST#, PLOCK# SMIACT# Valid Delay	2	24	ns	15-6	
t_9	BLAST#, PLOCK# Float Delay		28	ns	15-7	3
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	2	20	ns	15-6	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		28	ns	15-7	3
t_{12}	EADS# Setup Time	8		ns	15-3	
t_{13}	EADS# Hold Time	3		ns	15-3	
t_{14}	KEN#, BS16#, BS8# Setup Time	8		ns	15-3	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	15-3	
t_{16}	RDY#, BRDY# Setup Time	8		ns	15-4	
t_{17}	RDY#, BRDY# Hold Time	3		ns	15-4	
t_{18}	HOLD, AHOLD Setup Time	8		ns	15-3	
t_{18a}	BOFF# Setup Time	8		ns	15-3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	15-3	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# SRESET, STPCLK#, SMI# Setup Time	8		ns	15-3	5
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE# SRESET, STPCLK#, SMI# Hold Time	3		ns	15-3	5
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	15-3, 15-4	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	15-3, 15-4	

NOTES:
1. V_{CC5} should be connected to 3.3V ±5% in 3.3V-only systems.
2. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant Acknowledge protocol is used.
3. Not 100% tested. Guaranteed by design characterization.
4. All timing specifications assume C_L = 50 pF. See capacitive derating charts for additional timing delays due to loading.
5. A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.
6. For adjacent clocks, assumes frequency of operation is constant. STPCLK# input should be used to change frequency of operation.

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Table 15-9. 3.3V AC Characteristics for the 100/33-MHz IntelDX4™ Processors

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	CLK Frequency	8	33	MHz		2
t_1	CLK Period	30	125	ns	15-2	
t_{1a}	CLK Period Stability		±250	ps		3, 6
t_2	CLK High Time	11		ns	15-2	at 2V
t_3	CLK Low Time	11		ns	15-2	at 0.8V
t_4	CLK Fall Time		3	ns	15-2	2V to 0.8V
t_5	CLK Rise Time		3	ns	15-2	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA Valid Delay	2	14	ns	15-6	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		20	ns	15-7	3
t_8	PCHK# Valid Delay	2	14	ns	15-5	
t_{8a}	BLAST#, PLOCK#, SMIACT# Valid Delay	2	14	ns	15-6	
t_9	BLAST#, PLOCK# Float Delay		20	ns	15-7	3
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	2	14	ns	15-6	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		20	ns	15-7	3
t_{12}	EADS# Setup Time	5		ns	15-3	
t_{13}	EADS# Hold Time	3		ns	15-3	
t_{14}	KEN#, BS16#, BS8# Setup Time	5		ns	15-3	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	15-3	
t_{16}	RDY#, BRDY# Setup Time	5		ns	15-4	
t_{17}	RDY#, BRDY# Hold Time	3		ns	15-4	
t_{18}	HOLD, AHOLD Setup Time	6		ns	15-3	
t_{18a}	BOFF# Setup Time	7		ns	15-3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	15-3	

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Table 15-9. 3.3V AC Characteristics for the 100/33-MHz IntelDX4™ Processors (Continued)

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, SRESET, STPCLK#, SMI# Setup Time	5		ns	15-3	5
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, IGNNE#, SRESET, STPCLK#, SMI# Hold Time	3		ns	15-3	5
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	15-3, 15-4	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	15-3, 15-4	

NOTES:
1. V_{CC5} should be connected to 3.3V ±5% in 3.3V-only systems.
2. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant Acknowledge protocol is used.
3. Not 100% tested. Guaranteed by design characterization.
4. All timing specifications assume C_L = 50 pF. See capacitive derating charts for additional timing delays due to loading.
5. A reset pulse width of 15 CLK cycles is required for warm resets (RESET or SRESET). Power-up resets (cold resets) require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.
6. For adjacent clocks, assumes frequency of operation is constant. STPCLK# input should be used to change frequency of operation.

Table 15-10. 3.3V IntelDX4™ Processor AC Specifications for the Test Access Port (All IntelDX4 Processor Frequencies)

V_{CC} = 3.3V ±5%; V_{CC5} = 5V ±0.25V (Note 1); T_{CASE} = −55°C to +125°C; C_L = 0 pF

Symbol	Parameter	Min	Max	Unit	Figure
t_{24}	TCK Frequency		25	MHz	
t_{25}	TCK Period	40		ns	
t_{26}	TCK High Time	10		ns	
t_{27}	TCK Low Time	10		ns	
t_{28}	TCK Rise Time		4	ns	
t_{29}	TCK Fall Time		4	ns	
t_{30}	TDI, TMS Setup Time	8		ns	15-8
t_{31}	TDI, TMS Hold Time	7		ns	15-8
t_{32}	TDO Valid Delay	3	25	ns	15-8
t_{33}	TDO Float Delay		30	ns	
t_{34}	All Outputs (Non-Test) Valid Delay	3	25	ns	15-8
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	15-8
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	15-8
t_{37}	All Inputs (Non-Test) Hold Time	7		ns	15-8

NOTES:
1. V_{CC5} should be connected to 3.3V ±5% in 3.3V-only systems.
2. All inputs and outputs are TTL Level.
3. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
4. TCK period ≤ CLK period.
5. Parameters t_{30}–t_{37} are measured from TCK.

15.4.2 5V AC CHARACTERISTICS

Table 15-11 is for 25- and 33-MHz Military Intel486 DX, 50-MHz IntelDX2™ (25-MHz Max.) and 66-MHz IntelDX2 (33-MHz Max.) processors.

Table 15-11. 5V AC Characteristics

Functional operating range: V_{CC} = 5V ±0.25V; T_{CASE} = −55°C to +125°C; C_L = 50 pF unless otherwise specified. (See also Table 15-12).

Symbol	Parameter	Bus Speed				Unit	Figure	Notes
		25 MHz		33 MHz				
		Min	Max	Min	Max			
	Frequency	8	**25**	8	**33**	MHz		1
t_1	CLK Period	40	125	30	125	ns	15-2	
t_{1a}	CLK Period Stability		±250		±250	ps	15-2	Adjacent clocks(2)
t_2	CLK High Time	14		11		ns	15-2	at 2V
t_3	CLK Low Time	14		11		ns	15-2	at 0.8V(2)
t_4	CLK Fall Time		4		3	ns	15-2	2V to 0.8V(2)
t_5	CLK Rise Time		4		3	ns	15-2	0.8V to 2V(2)
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA, SMIACT#, FERR# Valid Delay	2	19	2	16	ns	15-6	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, BREQ, HLDA Float Delay		28		20	ns	15-7	2
t_8	PCHK# Valid Delay	2	24	2	22	ns	15-5	
t_{8a}	BLAST#, PLOCK# Valid Delay	2	24	2	20	ns	15-6	
t_9	BLAST#, PLOCK# Float Delay		28		20	ns	15-7	2
t_{10}	D0–D31, DP0–DP3 Write Data Valid Delay	2	20	2	18	ns	15-6	
t_{11}	D0–D31, DP0–DP3 Write Data Float Delay		28		20	ns	15-7	2
t_{12}	EADS# Setup Time	8		5		ns	15-3	
t_{13}	EADS# Hold Time	3		3		ns	15-3	
t_{14}	KEN#, BS16#, BS8# Setup Time	8		5		ns	15-3	

Table 15-11. 5V AC Characteristics (Continued)
Functional operating range: V_{CC} = 5V ±0.25V; T_{CASE} = −55°C to +125°C; C_L = 50 pF unless otherwise specified.

Symbol	Parameter	Bus Speed				Unit	Figure	Notes
		25 MHz		33 MHz				
		Min	Max	Min	Max			
t_{15}	KEN#, BS16#, BS8# Hold Time	3		3		ns	15-3	
t_{16}	RDY#, BRDY# Setup Time	8		5		ns	15-4	
t_{17}	RDY#, BRDY# Hold Time	3		3		ns	15-4	
t_{18}	HOLD, AHOLD Setup Time	10		6		ns	15-3	
t_{18a}	BOFF# Setup Time	10		8		ns	15-3	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		3		ns	15-3	
t_{20}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Setup Time	10		5		ns	15-3	
t_{21}	FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, RESET, IGNNE# Hold Time	3		3		ns	15-3	
t_{22}	D0–D31, DP0–DP3, A4–A31 Read Setup Time	5		5		ns	15-3 15-4	
t_{23}	D0–D31, DP0–DP3, A4–A31 Read Hold Time	3		3		ns	15-3 15-4	

NOTES:
1. 0-MHz operation is guaranteed when the STPCLK# and Stop Grant bus cycle protocol is used.
2. Not 100% tested, guaranteed by design characterization.

Table 15-12. 5V Military Intel486 Processor AC Specifications for the Test Access Port (All Processors and Frequencies)

V_{CC} = 5V ±0.25V; T_{CASE} = −55°C to +125°C; C_L = 50 pF

Symbol	Parameter	Min	Max	Unit	Notes
t_{24}	TCK Frequency		8	MHz	1
t_{25}	TCK Period	125		ns	
t_{26}	TCK High Time	40		ns	@ 2.0V
t_{27}	TCK Low Time	40		ns	@ 0.8V
t_{28}	TCK Rise Time		8	ns	2
t_{29}	TCK Fall Time		8	ns	2
t_{30}	TDI, TMS Setup Time	8		ns	3
t_{31}	TDI, TMS Hold Time	10		ns	3
t_{32}	TDO Valid Delay	3	30	ns	3
t_{33}	TDO Float Delay		36	ns	3
t_{34}	All Outputs (Non-Test) Valid Delay	3	30	ns	3
t_{35}	All Outputs (Non-Test) Float Delay		36	ns	3
t_{36}	All Inputs (Non-Test) Setup Time	8		ns	3
t_{37}	All Inputs (Non-Test) Hold Time	10		ns	3

NOTES:
1. TCK period ≤ CLK period.
2. Rise/Fall times are measured between 0.8V and 2.0V. Rise/Fall times can be relaxed by 1 ns per 10-ns increase in TCK period.
3. Parameters t_{30}–t_{37} are measured from TCK.
4. Refer to Figure 15-18 for signal waveforms.

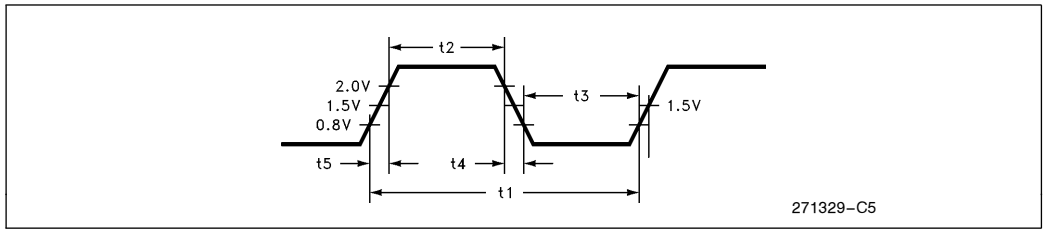


Figure 15-2. CLK Waveforms

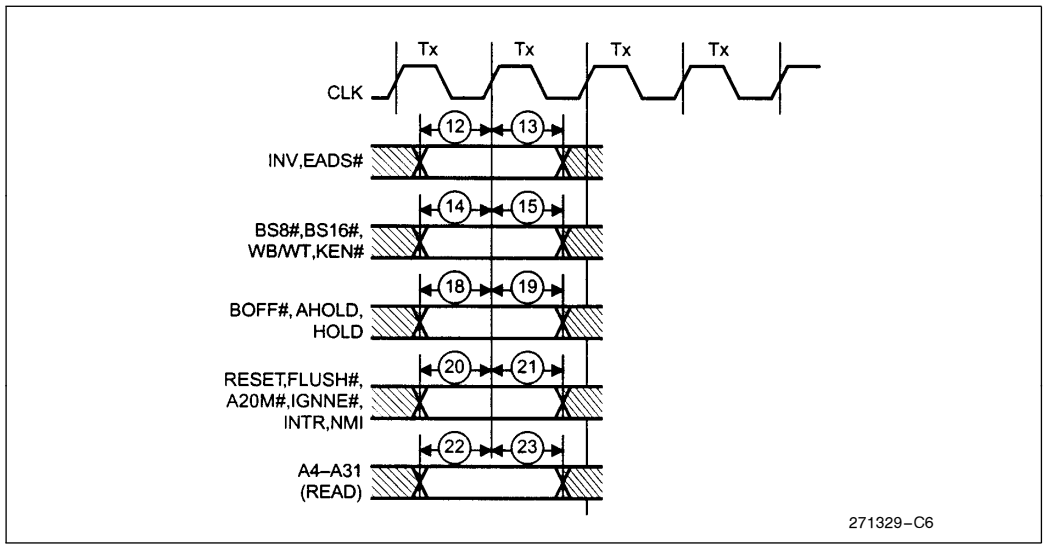


Figure 15-3. Input Setup and Hold Timing

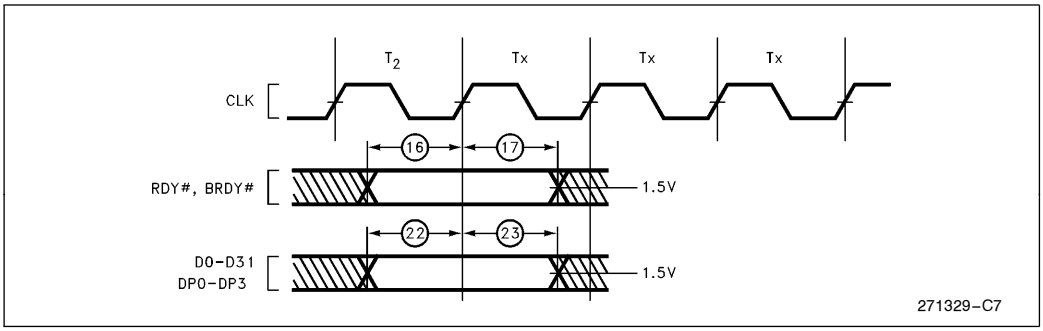


Figure 15-4. Input Setup and Hold Timing

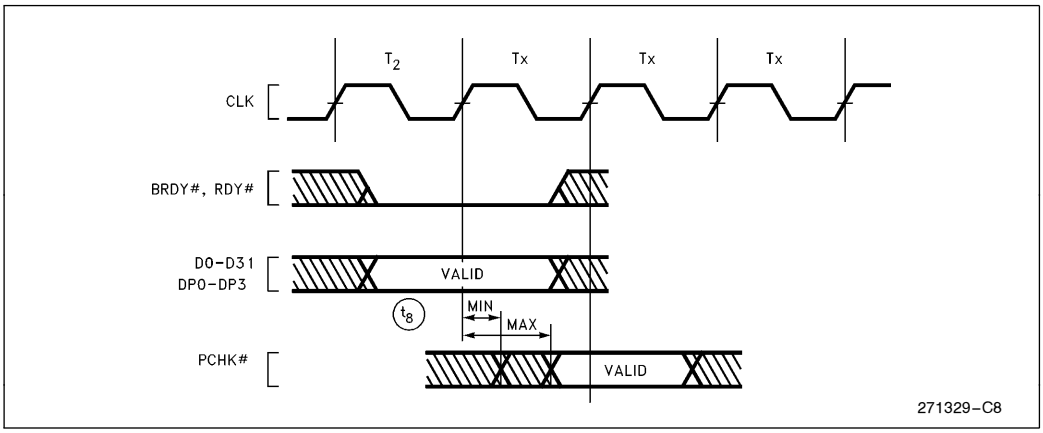


Figure 15-5. PCHK# Valid Delay Timing

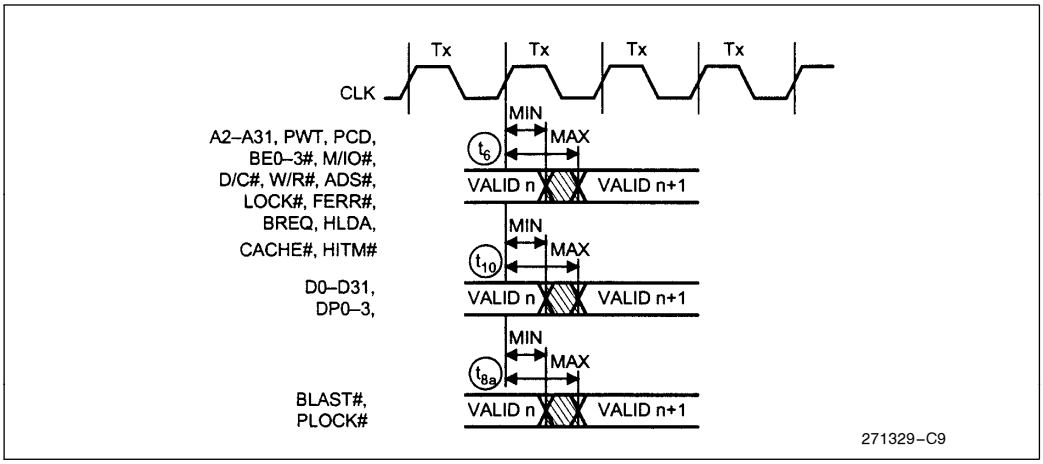


Figure 15-6. Output Valid Delay Timing

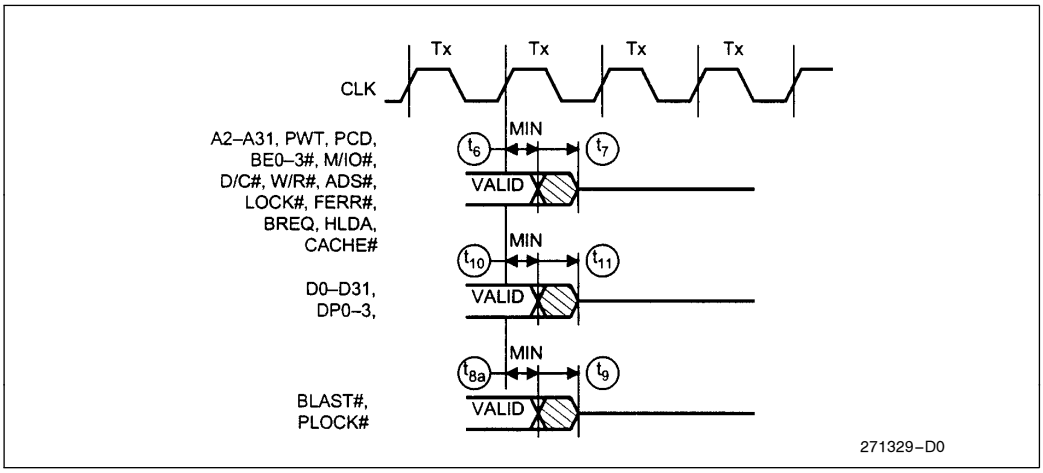


Figure 15-7. Maximum Float Delay Timing

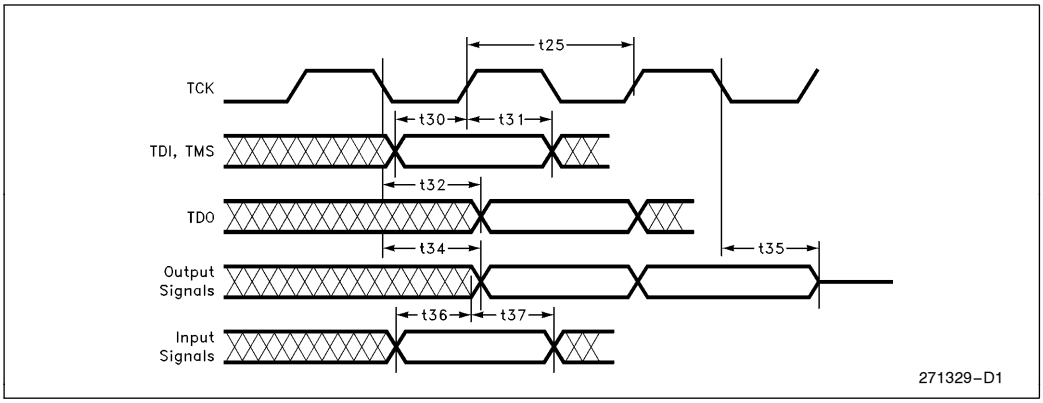
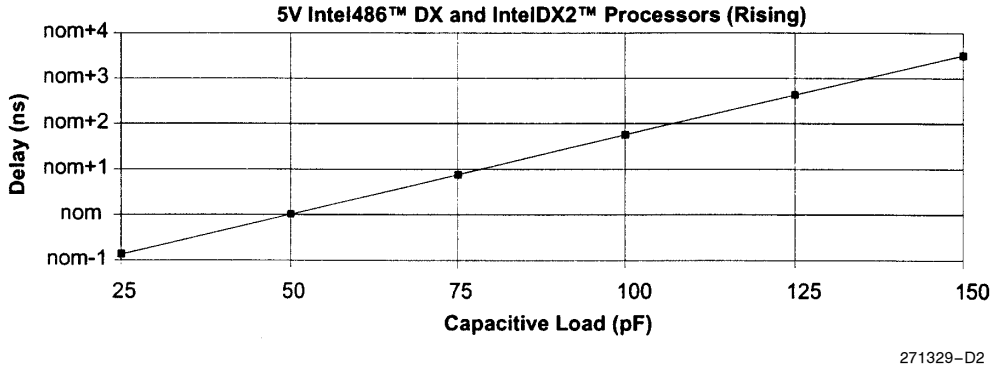


Figure 15-8. Test Signal Timing Diagram

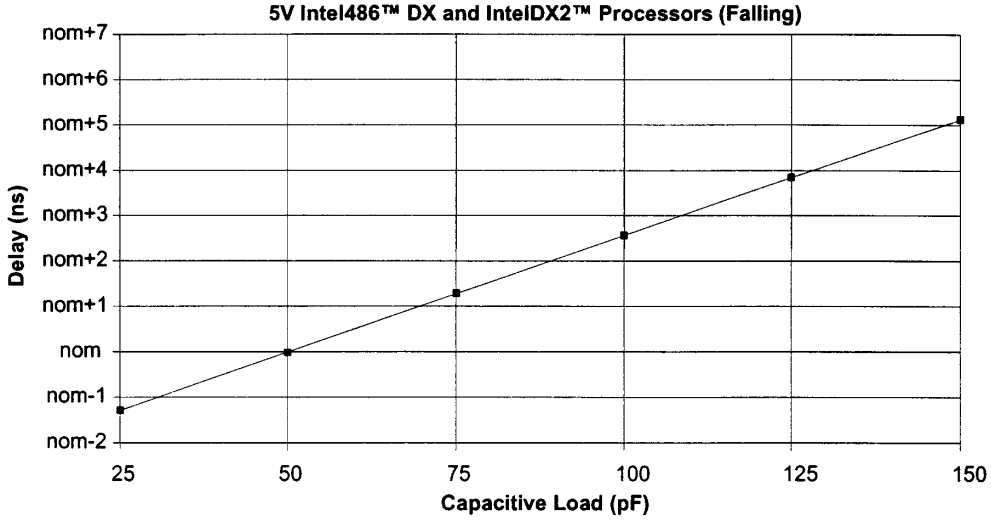
15.5 Capacitive Derating Curves

The capacitive derating curves illustrate output delay versus capacitive load for 5V Military Intel486 processors. The derating curves show the delays for the rising and falling edges under worst-case conditions. Figure 15-9 and Figure 15-10 apply to 5V Military Intel486 DX and IntelDX2 processors. Figures 15-11, 15-12 and 15-13 apply to the IntelDX4 processor. The figures apply to all frequencies specified for each corresponding product. Refer to Appendix B for bus frequencies above 33 MHz for Military Intel486 processors.



NOTE:
This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 15-9. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a Low-to-High Transition



NOTE:
This graph will not be linear outside of the capacitive range shown.
nom = nominal value from the AC Characteristics table.

Figure 15-10. Typical Loading Delay versus Load Capacitance under Worst-Case Conditions for a High-to-Low Transition

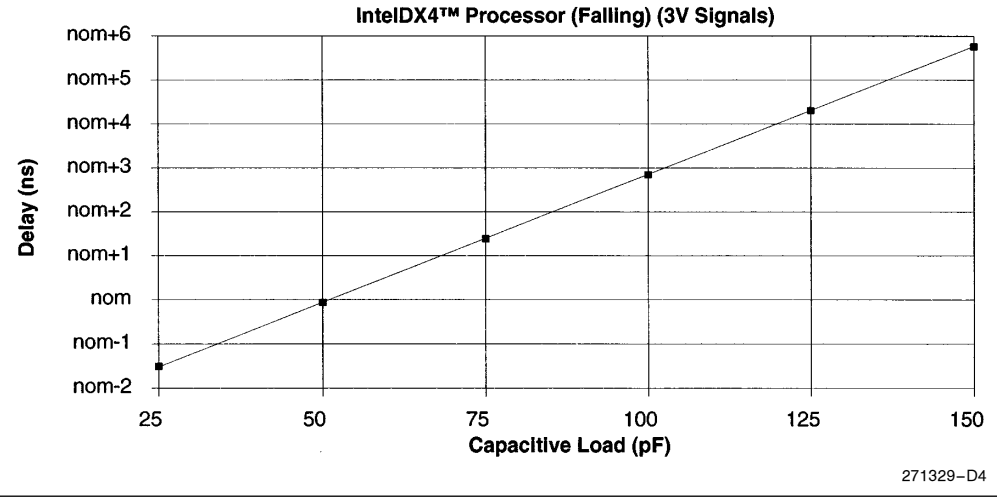


Figure 15-11. IntelDX4™ Processor Capacitive Derating Curve for High-to-Low Transitions (3V Signals)

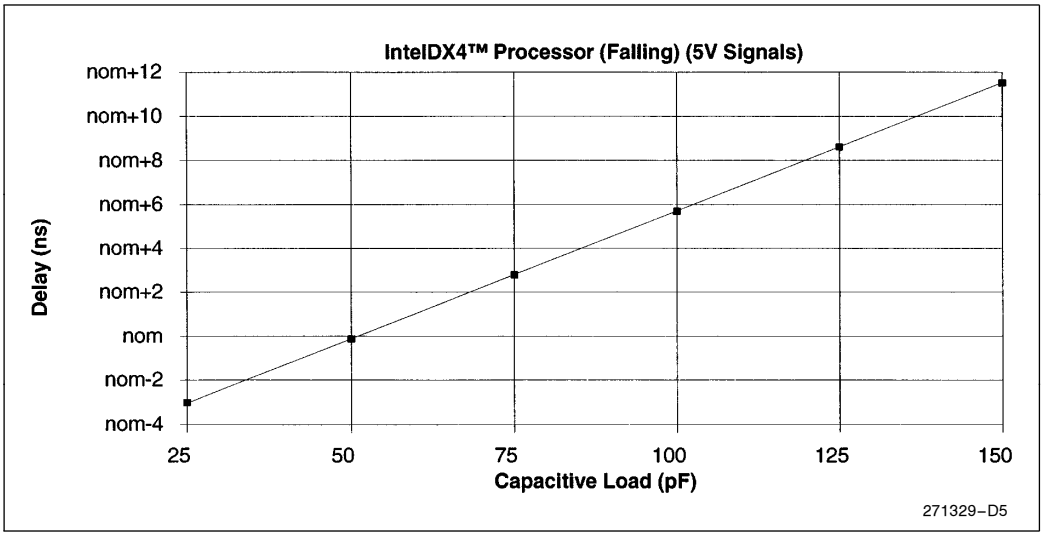


Figure 15-12. IntelDX4™ Processor Capacitive Derating Curve for Low-to-High Transitions (5V Signals)

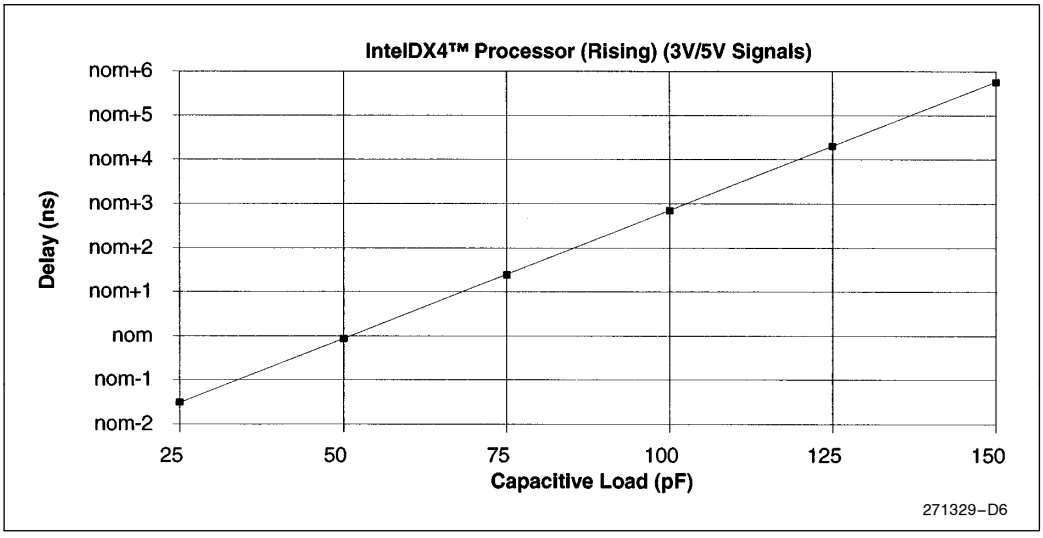


Figure 15-13. IntelDX4™ Processor Capacitive Derating Curve for Low-to-High Transitions (3V/5V Signals)

16.0 MECHANICAL DATA

This section describes the package dimensions and thermal specifications for all processors in the Military Intel486 processor family.

NOTE:
For further details about thermal and mechanical package specifications and methodologies, refer to the 1994 Packaging Handbook (order number 240800).

16.1 Military Intel486 Processor Package Dimensions

The processor dimensions are listed in the following order:

- 168-pin PGA package;
- 196-lead PQFP package.

16.1.1 168-PIN PGA PACKAGE

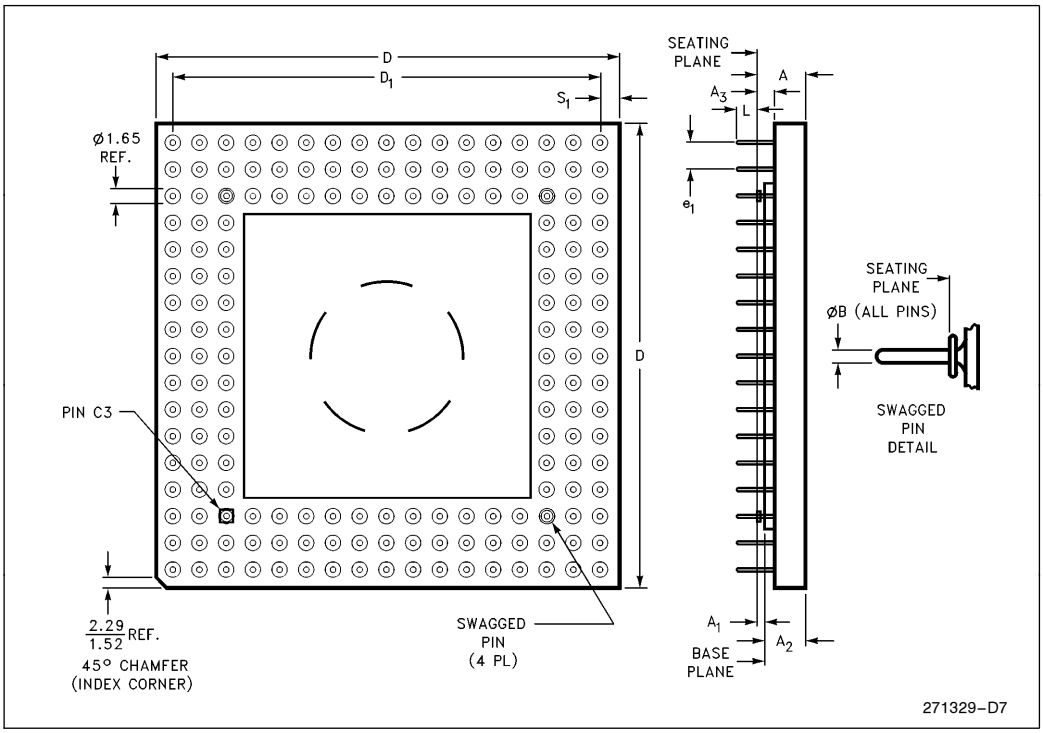


Figure 16-1. 168-Pin Ceramic PGA Package Dimensions

Table 16-1. 168-Pin Ceramic PGA Package Dimensions

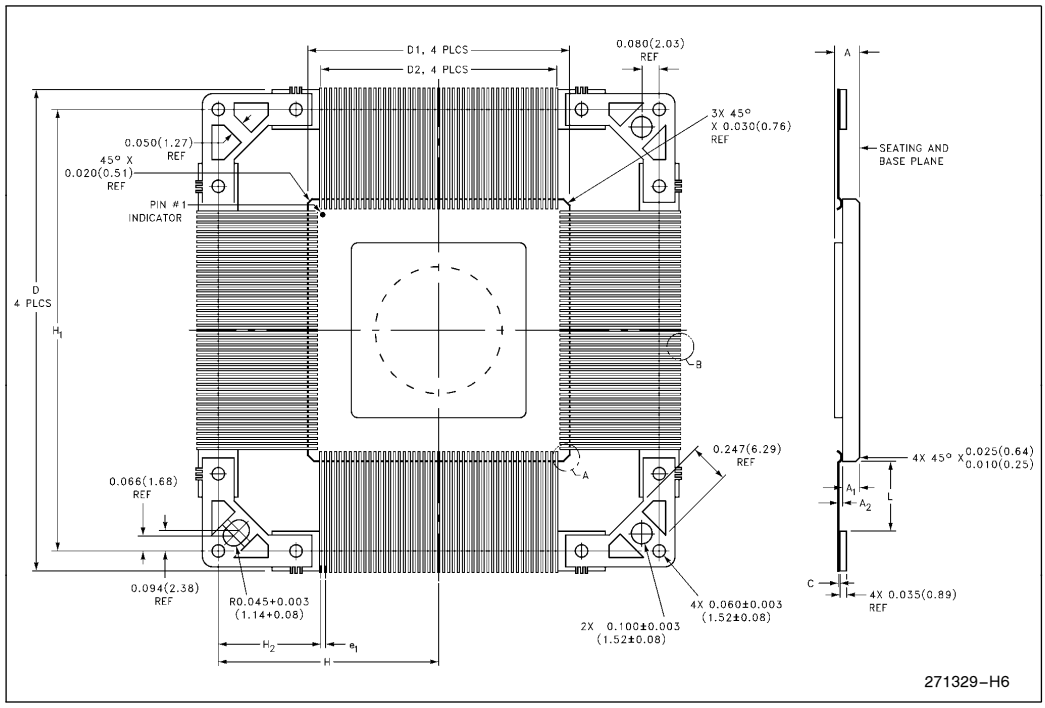
Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	SOLID LID	0.025	0.045	SOLID LID
A_2	2.8	3.5	SOLID LID	0.110	0.140	SOLID LID
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		0.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168			168		
S_1	1.52	2.54		0.060	0.100	
ISSUE	IWS REV X 7/15/88					

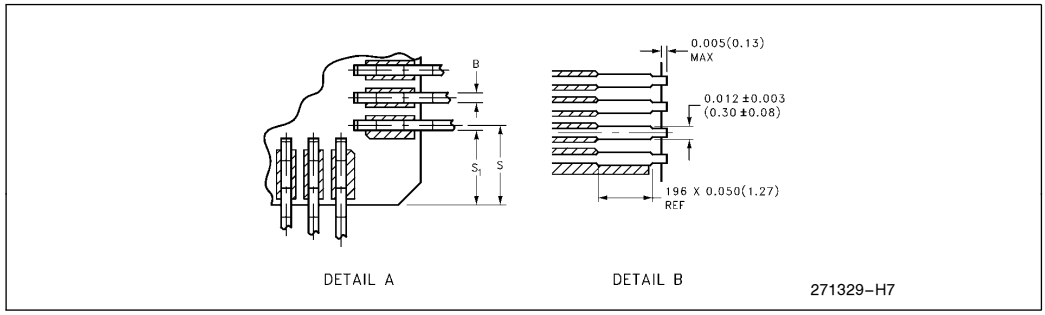
Table 16-2. Ceramic PGA Package Dimension Symbols

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane (lid)
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S_1	Other body dimension, outer lead center to edge of body

NOTES:
1. Controlling dimension: millimeter.
2. Dimension ''e_1'' (''e'') is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions ''B'', ''B_1'' and ''C'' are nominal.
5. Details of Pin 1 identifier are optional.

196L CERAMIC QUADPACK PACKAGE INTEL TYPE Q CAVITY UP, WITH N/C TIE BAR





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196L CERAMIC QUADPACK PACKAGE INTEL TYPE Q CAVITY UP, WITH N/C TIE BAR (Continued)

Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	2.23	2.92	Solid Lid	0.088	0.115	Solid Lid
A	2.92	3.56	EPROM Lid	0.115	0.140	EPROM Lid
A_1	1.96	2.39		0.077	0.094	
A_2	0.15	0.30		0.006	0.012	
B	0.20	0.25		0.008	0.010	
C	0.10	0.20		0.004	0.008	
D	62.99	64.01		2.480	2.520	
D_1	33.65	34.16		1.325	1.345	
D_2	30.48 Basic			1.200 Basic		
e_1	0.58	0.69		0.023	0.027	
H	29.21 Basic			1.150 Basic		
H_1	58.42 Basic			2.30 Basic		
H_2	13.97 Basic			0.550 Basic		
L	9.27	10.03		0.365	0.395	
N	196			196		
S	1.27	2.03	Reference	0.050	0.080	Reference
S_1	1.14	1.93	Reference	0.045	0.076	Reference
ISSUE	IWS 7/90					

16.2 Package Thermal Specifications

The Military Intel486 processors are specified for operation when T_C (the case temperature) is within the range of 0°C–85°C. T_C may be measured in any environment to determine whether the Military Intel486 processor is within the specified operating range. The case temperature, with and without heat sink should be measured using a 0.005″ diameter (AWG#36) thermocouple with a 90° angle adhesive bond at the center of the package top surface, opposite the pins. Figure 16-2 and Figure 16-3 illustrate this methodology.

The ambient temperature (T_A) is guaranteed as long as T_C is not violated. The ambient temperature can be calculated from θ_{JC} and θ_{JA} from the following equations.

$$T_J = T_C + P * \theta_{JC}$$
$$T_A = T_J - P * \theta_{JA}$$
$$T_C = T_A + P * [\theta_{JA} - \theta_{JC}]$$

Where:

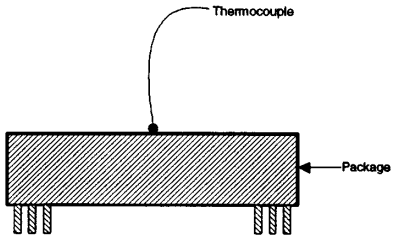
T_J, T_A, T_C = Junction, Ambient and Case Temperature, respectively.

θ_{JC}, θ_{JA} = Junction-to-Case and Junction-to-Ambient thermal Resistance, respectively.

P = Maximum Power Consumption

The values for θ_{JA} and θ_{JC} are given below for the packaging and operating frequencies.

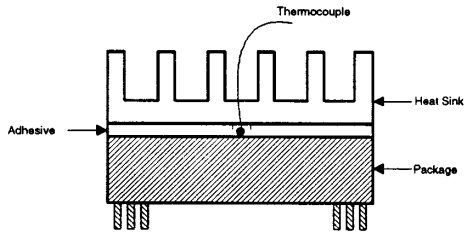
Note that T_A is greatly improved by attaching ''fins'' or a ''heat sink'' to the package. P (the maximum power consumption) is calculated by using the maximum I_{CC} at nominal V_{CC} (either 3.3V or 5V) as tabulated in the DC Charisteristics in section 15.



271329–D8

0.005″ diam. thermocouple on the center of the package top surface with a 90° angle adhesive bond

Figure 16-2. Case Temperature Measurement without Heat Sink

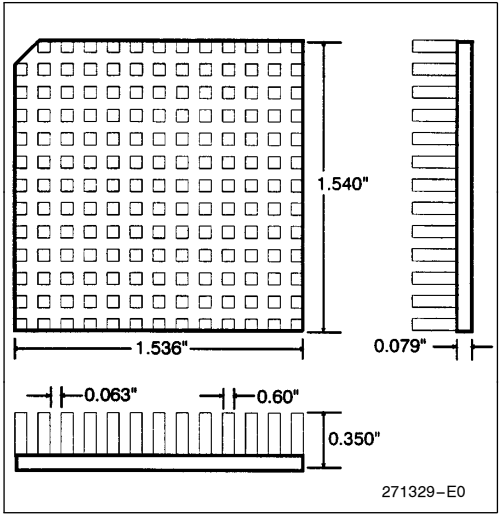


271329–D9

0.005″ diam. thermocouple on the center of the package top surface with a 90° angle adhesive bond through a hole drilled at the heat sink base

Figure 16-3. Case Temperature Measurement with Heat Sink

16.2.1 168-PIN PGA PACKAGE THERMAL CHARACTERISTICS FOR 3.3V IntelDX4 PROCESSOR



271329–E0

Figure 16-4. Sample IntelDX4™ Processor PGA Heat Sink

Table 16-3. PGA Package Thermal Resistance (°C/W)–θ_{JC} and θ_{JA} for IntelDX4™ Processor

		θ_{JA} vs Airflow—ft/min (m/sec)					
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
With Heat Sink*	2	13.5	8.5	6.5	5.5	4.5	4.25
Without Heat Sink	2	17.5	15	13	11.5	10.0	9.5

*0.350″ high omnidirectional heat sink.

Table 16-4. PGA Package Maximum Ambient Temperature for IntelDX4™ Processor

		Airflow—ft/min (m/sec)			
	Freq. (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
$T_{ambient}$ °C with Heat Sink*	100	35.5	57	65.5	70
$T_{ambient}$ °C without Heat Sink	100	18.5	29	37.5	44

*0.350″ high omnidirectional heat sink.

16.2.2 168-Pin PGA Package Thermal Characteristics for 5V Military Intel486 Processors

Table 16-5. Thermal Resistance (°C/W) θ_{JC} and θ_{JA} for the 168-Pin PGA Package of the Military Intel486™ Processor

		θ_{JA} vs. Airflow—ft/min. (m/sec)					
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
With Heat Sink*	1.5	13	8.0	6.0	5.0	4.5	4.25
Without Heat Sink	1.5	17	14.5	12.5	11.0	10.0	9.5

*0.350″ high omnidirectional heat sink.

16.2.3 Thermal Specifications for 196-Lead CQFP Package

Table 16-6. Thermal Resistance (°C/W) °JC and °JA

		θ_{JA} vs Airflow—ft/min (m/sec)			
	θ_{JC}	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)
With Heat Sink*	2.5	17.0	10.5	8.5	8.0
Without Heat Sink	2.5	20.5	16.5	14.0	12.5

*0.350″ high omnidirectional heat sink.